CLAIMS

What is claimed is:

1. A method comprising:

ceasing bus access, in a configurable system on a chip, upon the occurrence of a specified event;

allowing completion of all pending bus transactions;

stopping the system clock such that the state of the hardware is held static; and

accessing the static state of the hardware through a debug port.

2. The method of claim 1, wherein the bus is a pipeline bus.

3. The method of claim 1, wherein the debug port is a bus master.

4. The method of claim 1, wherein allowing completion of all pending bus transactions includes monitoring the bus for pending bus transactions.

5. The method of claim 4, wherein allowing completion of all pending bus transactions further includes generating a qualified clock freeze cycle upon completion of all pending bus transactions.

6. The method of claim 1, wherein the specified event is programmed by a user.

7. A machine-readable medium that provides executable instructions, which when executed by a processor, cause said processor to perform a method comprising:

ceasing bus access, in a configurable system on a chip, upon the occurrence of a specified event;

allowing completion of all pending bus transactions;

stopping the system clock such that the state of the hardware is held static; and

accessing the static state of the hardware through a debug port.

8. The machine-readable medium of claim 7, wherein the bus is a pipeline bus.

9. The machine-readable medium of claim 7, wherein the debug port is a bus master.

10. The machine-readable medium of claim 7, wherein allowing completion of all pending bus transactions includes monitoring the bus for pending bus transactions.

11. The machine-readable medium of claim 10, wherein allowing completion of all pending bus transactions further includes generating a qualified clock freeze cycle upon completion of all pending bus transactions.

12. The machine-readable medium of claim 7, wherein the specified event is programmed by a user.

13. An apparatus comprising:

means to cease bus access, in a configurable system on a chip, upon the occurrence of a specified event;

means to allow completion of all pending bus transactions;

means to stop the system clock such that the state of the hardware is held static; and

means to access the static state of the hardware through a debug port.

14. The apparatus of claim 13, wherein the bus is a pipeline bus.

15. The apparatus of claim 13, wherein the debug port is a bus master.

16. The apparatus of claim 13, wherein allowing completion of all pending bus transactions includes monitoring the bus for pending bus transactions.

17. The apparatus of claim 16, wherein allowing completion of all pending bus transactions further includes generating a qualified clock freeze cycle upon completion of all pending bus transactions.

18. The apparatus of claim 13, wherein the specified event is programmed by a user.